REMARKS

1. Claims 1-13are pending and stand rejected.

Reconsideration of this application is respectfully requested.

2. The drawings stood objected to because in the previous Office Action mailed on June 13, 2005 because they did not include reference numeral 403 mentioned in the specification; FIG. 3 included reference numerals not mentioned in the specification; and FIGS. 1 and 2 were not designated prior art.

In the amendment and response filed on September 15, 2005, drawing replacement sheets correcting the defects in FIGS. 1, 2 and 3 were submitted for the examiner's approval. The current Office Action does not indicate whether these drawing corrections have been approved. It is respectfully requested that the examiner indicate whether these drawing corrections have been approved in the next communication.

3. Claims 1-13 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 8-15 of U.S. Patent No. 6,933,198 to Chu et al. (Chu) in view of U.S. Patent 6,800,525 to Ryu et al. (Ryu). This rejection is respectfully traversed.

Independent claim 1 of the present application recites:

> A method of forming a split gate field effect transistor, comprising:
>
> providing a substrate having a pair of floating gate layer portions, a first conductive material layer between said pair of floating gate layer portions, and a first dielectric layer above said first conductive material layer;
>
> forming a pair of floating gates from said pair of floating gate layer portions using the first dielectric layer as a first etching hard mask;
>
> forming a control gate having a second dielectric layer above said control gate, wherein said control gate is self-aligned to said pair of floating gates by using said first and second dielectric layers as a second etching hard mask; and

forming a pair of source/drain regions into said substrate and beside said pair of floating gates and said control gate.

Independent claim 8 of Chu, on the other hand, recites:

A method for forming a split gate field effect transistor device comprising:

providing a semiconductor substrate;

forming upon the semiconductor substrate a tunneling dielectric layer;

forming upon the tunneling dielectric layer a blanket floating gate electrode material layer;

forming upon the blanket floating gate electrode material layer a thermal oxidation stop layer;

forming upon the thermal oxidation stop layer a blanket silicon layer;

forming upon the blanket silicon layer a patterned mask layer;

thermally oxidizing the blanket silicon layer to form a patterned silicon oxide layer which encroaches beneath the patterned mask layer;

etching the blanket floating gate electrode material layer to form a floating gate electrode while employing the patterned silicon oxide layer as an etch mask layer;

forming upon the floating gate electrode an intergate electrode dielectric layer; and

forming upon the intergate electrode a control gate electrode.

Claim 1 of the present application calls for features which are not recited in claim 8 or any of claims 9-15 including forming a control gate having a second dielectric layer above the control gate, the control gate being self-aligned to the pair of floating gates by

using the first and second dielectric layers as a second etching hard mask, and forming a pair of source/drain regions into the substrate beside the pair of floating gates and the control gate.

The examiner asserts that Ryu teaches the claimed control gate and source/drain forming steps not claimed by Chu. This assertion is respectfully traversed with respect to the claimed control gate forming step. Neither Chu nor Ryu teach or suggest that the silicon oxide layer recited in claim 8 of Chu (alleged to be the first dielectric layer by the examiner) can be used as a second etching hard mask. Ryu merely teaches a dielectric layer 217 disposed above the control gate. Chu teaches in column 8, lines 21-34, that the silicon oxide layers 34a-34d are used as an etch mask to pattern the thermal oxidation stop layer 28. After patterning the stop layer 28, the silicon oxide layers 34a-34d are removed and the patterned stop layers 28a-28d are used as a mask for etching the blanket floating gate electrode material layer 26. The control gate electrode is then formed further on in the process. Hence, Chu teaches that the control gate electrode is formed after the silicon oxide layers 34a-34d have been removed. Nothing in Chu or Ryu teaches or suggests that the control gate recited in claims 8-15 of Chu is self-aligned to the pair of floating gates by using the silicon oxide layers 34a-34d in Chu as part of a second etching hard mask, as recited in claim 1.

Claim 1 is, therefore, patentable over claims 8-15 of Chu in view of Ryu. Claims 2-13 are patentable over claims 8-15 of Chu in view of Ryu for at least the same reasons as set forth with respect to claim 1. In addition, claims 2-13 call for additional features which are not claimed in claims 8-15 of Chu in view of Ryu.

Accordingly, withdrawal of this rejection is respectfully urged.

4. Favorable reconsideration of this application is respectfully requested as it is believed that all outstanding issues have been addressed herein and, further, that claims 1-13 are in condition for allowance. Should there be any questions or matters whose resolution may be advanced by a telephone call, the examiner is cordially invited to contact applicants' undersigned attorney at his number listed below.

5. The Commissioner is hereby authorized to charge payment of any additional filing fees required under 37 CFR 1.16 and any patent application processing fees under 37 CFR 1.17, which are associated with this communication, or credit any overpayment to Deposit Account No. 50-2061.

Respectfully submitted,

Paul A. Schwarz
Registration No. 37,577

Duane Morris LLP
P.O. Box 5203
Princeton, NJ 08543-5203
609-631-2446– Tel
609-631-2401 – Fax